CHIP TO CHIP INTERFACE

Abstract

A chip to chip interface comprises a driver configured to receive a data signal and provide an output signal at a first level in response to receiving an odd number of consecutive logic highs in the data signal, at a second level in response to receiving an odd number of consecutive logic lows in the data signal, at a third level in response to receiving an even number of consecutive logic highs in the data signal and at a fourth level in response to receiving an even number of consecutive logic lows in the data signal.